CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of slave delay lock loops (DLLs) in a memory interface to adjust timing between a plurality of signals to compensate for timing skew; and

a plurality of input/output (I/O) buffers to output the plurality of signals to one or more memory devices coupled to the memory interface after adjusting the timing.

2. The apparatus of claim 1, further comprising a plurality of programmable configuration bits, coupled to the plurality of slave DLLs, to set an amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals.

3. The apparatus of claim 2, further comprising a slave DLL to adjust timing of a core clock signal in response to the amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals to generate a memory clock signal.

4. The apparatus of claim 1, further comprising a master DLL, coupled to the plurality of slave DLLs, to calibrate the plurality of slave DLLs.

5. The apparatus of claim 1, further comprising a plurality of multiplexers to couple each of the plurality of slave DLLs to one or more of the plurality of I/O buffers.

6. The apparatus of claim 1, further comprising a plurality of clock trees, each of the plurality of clock trees having a root coupled to an output of each of the plurality of slave DLLs, to clock each of the plurality of I/O buffers.

7. The apparatus of claim 1, wherein the plurality of signals includes a plurality of memory control signals.

8. A method comprising:

adjusting timing between a plurality of signals using a plurality of slave delay lock loops (DLLs) in a memory interface before sending the signals to one or more memory devices; and

sending the plurality of signals to the one or more memory devices.

9. The method of claim 8, wherein adjusting the timing comprises:

programming a plurality of configuration bits to set an amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals, the plurality of configuration bits being coupled to the plurality of slave DLLs.

10. The method of claim 9, further comprising adjusting timing of a core clock signal using a slave DLL in response to the amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals to generate a memory clock signal.

11. The method of claim 9, further comprising ting timing of a core clock signal in response to the plurality of configuration bits.

12. The method of claim 8, further comprising calibrating the plurality of slave DLLs using a master DLL.

13. The method of claim 8, further comprising clocking each of a plurality of input/output (I/O) buffers to output the plurality of signals in response to the amount of delay each of the plurality of slave DLLs applies to one of the plurality of signals.

14. The method of claim 8, wherein the plurality of signals includes a plurality of memory control signals.

15. A machine-accessible medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

programming a first plurality of configuration bits in a memory interface; and

causing a plurality of slave delay lock loops (DLLs) in the memory interface to adjust timing between a plurality of signals in response to the plurality of configuration bits before the plurality of signals are sent to one or more memory devices.

16. The machine-accessible medium of claim 15, wherein the operations further comprise:

programming a second plurality of configuration bits of a master DLL; and

causing the master DLL to calibrate the plurality of slave DLLs in response to the second plurality of configuration bits.

17. The machine-accessible medium of claim 16, wherein the operations further comprise programming a third plurality of configuration bits to adjust timing of a core clock signal using a slave DLL in response to the timing of the plurality of slave DLLs to generate a memory clock signal to be sent to the one or more memory devices.

18. A system comprising:

a graphics chip;

a plurality of memory devices; and

a memory controller coupled to the plurality of memory devices and the graphics chip, the memory controller having a memory interface that comprises

a plurality of slave delay lock loops (DLLs) to adjust timing between a plurality of signals to compensate for timing skew; and

a plurality of input/output (I/O) buffers to output the plurality of signals to one or more of the plurality of memory devices after adjusting the timing.

19. The system of claim 18, wherein the plurality of signals includes a plurality of memory control signals.

20. The system of claim 18, wherein the memory interface further comprises a master DLL to calibrate the plurality of slave DLLs, the master DLL is coupled to the plurality of slave DLLs.

21. The system of claim 18, further comprising a processor coupled to the memory controller.

22. The system of claim 18, wherein the plurality of memory devices includes a plurality of double-data rate (DDR) dynamic random access memory (DRAM) devices.